## REMARKS

This Amendment is submitted in response to the Office Action dated July 15, 2003, having a shortened statutory period set to expire October 15, 2003.

Pursuant to the Examiner's request in paragraph 3 of the present Office Action, Applicant has proposed amendments to the specification to provide a more descriptive title and to correct informalities in Table I on page 11. In addition, Applicant has canceled Claims 1-2 and amended Claim 13 to address the informalities in the claims noted by the Examiner in paragraphs 5-7.

In paragraph 9 of the present Office Action, Claims 1, 2, 10-11, and 13-15 are rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. US 5,396,604 to *DeLano et al.* (*DeLano*). In addition, in paragraph 18 of the present Office Action, Claims 3-8 are rejected under 35 U.S.C. § 103(a) as unpatentable over *DeLano* in view of *Tanenbaum,* "Structured Computer Organization, 2nd Edition", 1984 (*Tanenbaum*). In paragraph 25 of the present Office Action, Claim 9 is further rejected under 35 U.S.C. § 103(a) as unpatentable over *DeLano* in view of *Tanenbaum* and further in view of U.S. Patent No. US 5,931,957 to *Konigsburg et al.* (*Konigsburg*). In paragraph 27 of the present Office Action, Claim 12 is rejected under 35 U.S.C. § 103(a) as unpatentable over *DeLano*. In paragraph 29 of the present Office Action, Claim 16 is rejected under 35 U.S.C. § 103(a) as unpatentable over *DeLano* in view of *Konigsburg*. Those rejections are respectfully traversed, and favorable reconsideration of the claims is respectfully requested.

Applicant submits that the present claims are not rendered unpatentable by *DeLano*, whether considered alone or in combination with the other references of record, because the cited references do not individually or collectively teach or suggest each claim feature. For example, the combination of references do not teach or suggest a processor including:

> instruction processing circuitry that fetches an instruction sequence for execution..., wherein said instruction processing circuitry, after fetching said instruction sequence for execution and prior to dispatching said load instruction for execution and responsive to detecting said load instruction within said fetched instruction sequence, translates said load instruction into separately executable prefetch and register operations

as recited in exemplary Claim 3 (and similarly in Claim 10).

The Examiner acknowledges in paragraph 18 of the present Office Action that *DeLano* does not disclose the claimed "instruction processing circuitry" now recited in both Claims 3 and 10, and correctly notes that *DeLano* instead teaches the use of compiler software to insert prefetch instructions within an instruction stream in advance of a load instruction to prefetch data. The Examiner avers that the claimed "instruction processing circuitry" is nonetheless obvious in view of *Tanenbaum's* proposition, "Hardware and software are logically equivalent." That is, the Examiner argues that the conversion of *DeLano's* software compiler into hardware as taught by *Tanenbaum* would yield the instruction processing circuitry recited in Claims 3 and 10.

Applicant respectfully traverses the Examiner's position because the conversion of *DeLano's* software compiler into hardware (i.e. a hardware compiler) according to the teaching of *Tanenbaum* would not result in the claimed "instruction processing circuitry," which performs real-time instruction translation. That is, whether *DeLano's* compiler is realized in software (as taught by *DeLano*) or hardware (as allegedly suggested by *Tanenbaum*), *DeLano's* compiler operates by scanning an entire program prior to its execution, that is, off-line. The claimed "instruction processing circuitry," by contrast, translates the load instruction into separately executable prefetch and register operations "after fetching said instruction sequence for execution and prior to dispatching said load instruction for execution and responsive to detecting said load instruction within said fetched instruction sequence." That is, the claimed "instruction processing circuitry" translates the load instruction during program execution (as indicated by the recitation "after fetching said instruction sequence for execution and prior to dispatching said load instruction for execution"), advantageously avoiding the two-step compilation and execution process required by the Examiner's combination of references. Because the combination of references does not teach or suggest a modification to *DeLano's* compiler to permit it to be realized in hardware and function during program execution, Applicant submits that the combination of references does not render Claims 3 and 10 and their respective dependent claims unpatentable under 35 U.S.C. § 103.

Applicant further submits that Claims 7 and 14 are patentable over *DeLano* and *Tanenbaum* because that combination of references fails to disclose "said prefetch operation and

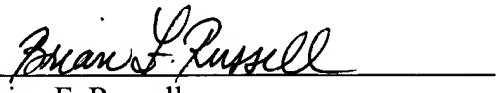
said register operation specify a same target register for said data and differ only in a value of a register operation field" as recited in Claims 7 and 14, as amended herein. In particular, as noted by the Examiner, *DeLano* explicitly teaches that the LOAD-to-GR0 instruction relied upon as teaching the claimed prefetch operation and the LOAD-to-GRx instruction relied upon as teaching the claimed register operation specify different target registers (*DeLano*, col. 5, line 46). As a result, *DeLano's* method of decreasing access latency can only be employed in processors supporting a LOAD-to-GR0 as a no-op (DeLano, col. 5, lines 39-40). Because *DeLano* does not disclose register and prefetch operations specifying a same target register, Applicant submits that the rejections of Claims 7 and 14 are overcome.

Applicant further submits that newly entered Claims 17-18 are patentable over *DeLano*, *Tanenbaum* and the other references of record because that cited references do not individually or collectively disclose "calculating a speculative target memory address utilizing contents of at least one register without regard for whether said contents will be modified between calculation of said speculative target memory address and performing said register operation." Upon careful review of the cited references, Applicant believes that speculative calculation of a target memory address is not disclosed by the cited references and therefore believes that Claims 17-18 are patentable over the prior art of record.

Having now responded to each objection and rejection set forth in the present Office Action, Applicant believes all pending claims are now in condition for allowance and respectfully requests such allowance.

No additional fee is believed to be required; however, in the event any additional fees are required, please charge IBM CORPORATION Deposit Account No. **09-0447**.

Respectfully submitted,



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